IN THE SPECIFICATION:

Page 2:

Please substitute the following paragraph for the first paragraph after "SUMMARY OF THE INVENTION":

The inventors have examined the circuit configuration of the LSI that has the same function and conforms to the two types of the external supply voltage specifications. The system that the inventors have examined will be outlined as follows.

Page 3:

Please substitute the following paragraph for the paragraph beginning at line 6:

Fig. 31 illustrates one example of the LSI circuit construction conforming to the supply voltage specifications shown in Fig. 29. The LSI (000) is composed of an input circuit (001), step-down circuit (002), internal circuit (101), and output circuit (003). The step-down circuit (002) lowers the external supply voltage (VDD) to the internal supply voltage (VDDI), which is supplied to the internal circuit (101). The input circuit (001) and the output circuit (003) are directly supplied with the input signal (IN) and the I/O supply voltage (VDDQ) that varies depending upon the external supply voltage specifications.

Page 6:

Please substitute the following paragraph for the paragraph beginning 3 lines from the bottom of the page:

In accordance with one aspect of the invention, the semiconductor device includes an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate, in which a spacing between a first gate electrode of the first MOS transistors constituting the input circuit or the output circuit and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the first gate electrode and the first contact hole, and a spacing between a second gate electrode of the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole.

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Page 15:

Please substitute the following paragraph for the paragraph beginning 3 lines from the bottom of the page:

Among the MOS transistors that constitute the data output circuit 104, the n-channel MOS transistors (f32, f34, f36) and the p-channel MOS transistors (f31, f33, f35, f37) are directly supplied with the I/O supply voltage (VDDQ) that differs depending on the external supply voltage specifications. Therefore, the MOS transistors (f31 to f37) formed on the silicon chip 1a are designed to withstand 2.5 V so as to exhibit the high-speed performance when the I/O supply voltage (VDDQ) of 2.5 V is supplied thereto. On the other hand, the MOS transistors (f31 to f37) formed on the silicon chip 1b are designed to withstand 3.3 V so as to exhibit the high-speed performance when the I/O supply voltage (VDDQ) of 3.3 V is supplied thereto. The other MOS transistors of the data output circuit 104 are designed to withstand 3.3 V for both the silicon chip 1a and 1b, so that they can be used with the two kinds of supply voltages (2.5 V, 3.3 V).

Page 17:

Please substitute the following paragraph for the paragraph beginning at line 6:

Fig. 7(a) is a plan view of the 3.3 V withstanding MOS transistor formed on the silicon chip 1b, and Fig. 7(b) is a plan view of the 1.5 V withstanding MOS transistor formed on the same silicon chip 1b. The 3.3 V withstanding MOS transistor and the 1.5 V withstanding MOS transistor each have the gate insulating film thickness (TOX) and the minimum processing gate length (Lg) as shown in Fig. 30. In the 3.3 V withstanding MOS transistor, the spacing between the gate electrode 8b and the contact hole 17 for connecting the source and drain regions to the wiring region is formed in the minimum processing dimension (a) of this spacing, in order to promote the microstructure. Also, in the 1.5 V withstanding MOS transistor, the spacing between the gate electrode 8c and the contact hole 16 for connecting the source and drain regions to the wiring region is formed in the minimum processing dimension (a) of this spacing, for the same reason.